WHAT IS CLAIMED IS:

1. A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer; and

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer.

2. The method of claim 1, further comprising forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.

3. The method of claim 2, wherein said non-insulating layer is an anti-reflective layer (ARL).

4. The method according to claim 3, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

5. The method according to claim 4, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

6. The method according to claim 5, wherein said thermal process is a rapid thermal oxidation is performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range of from 850°C to 1050°C.

7. The method according to claim 4, wherein said conformal insulating layer is formed by deposition.

8. The method of claim 3, wherein said ARL is an anti-reflective coating.

9. The method of claim 3, wherein said ARL is titanium nitride.

10. The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. The method according to claim 10, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

12. The method according to claim 2, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

13. A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric.

14. The method of claim 13, further comprising forming a non-insulating layer over at least a portion of the resultant structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer.

15. The method of claim 14, wherein said non-insulating layer is an anti-reflective layer (ARL).

16. The method according to claim 15, wherein said insulating layer is formed by deposition.

17. The method according to claim 16, wherein to forming said insulating layer by deposition, an anneal is performed.

18. The method according to claim 15, wherein said insulating layer is grown.

19. The method according to claim 15, wherein said insulating layer is an oxide layer with a thickness in the range of from 500Å to 2000Å.

20. The method according to claim 15, wherein said side wall spacers have a width in the range of from 500Å to 2000Å.

21. The method according to claim 15, wherein said ARL is an anti-reflective coating.

22. The method according to claim 15, wherein said ARL is titanium nitride.

23. The method according to claim 15, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

24. The method according to claim 23, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

25. The method according to claim 15, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

26. A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an anti-reflective layer (ARL) over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

27. The method according to claim 26, wherein said ARL is an anti-reflective coating.

28. The method according to claim 26, wherein said ARL is titanium nitride.

29. The method according to claim 26, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

30. The method according to claim 26, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.